REMARKS

In view of the preceding amendments and following remarks, reconsideration of the present application is respectfully requested.

Claims 1-20 were pending in the Application and were rejected. By this Response, Claims 1-20 are canceled, and Claims 21-22 are added. No new matter is introduced herein.

Claims 1, 10-12, and 16 were objected to. Claims 1-4, 7, 8, 10-14, 16, 17, and 19, were rejected under 35 USC 102(b) as being anticipated by Taylor. Claims 9 and 18 were rejected under 35 USC 103(a) as being unpatentable over Taylor. Claims 5, 6, 15, and 20, were rejected under 35 USC 103(a) as being unpatentable over Taylor.

The present invention relates to series voltage regulators and a novel way to reduce the current to ground that bypasses the load and is therefore wasted. The pending claims and the Specification evidently were not clear on how this is accomplished and why it's patentable over the cited prior art.

The problem existing in the prior art which is being addressed by the present invention is illustrated in Fig. 1. The load is represented by element 17. For example, a regulated voltage of about 40-volts is needed to power load 17. The power supply voltage available at node 13 is

several hundred volts, e.g., 650-volts. So JFET transistor 12 is used to step this voltage down by dropping it between the JFET-drain and JFET-source.

A fraction of the source-drain current will appear in the gate, since this is a junction type FET. Such fraction represents the multiplication factor of JFET 12, e.g., its beta. Such JFET-gate current is labeled 16. It sinks directly to ground and does no useful work because it does not flow through to the output load. Gate current 16 is not a constituent of load current 17.

It would be more efficient if the JFET-drain current 16 could be steered into load 17. This is exactly what the present invention does, and a working circuit is illustrated in Fig. 2. JFET 21 drops most of the voltage between its drain connected to voltage source 23 and its source connected to the drain of JFET 22. The gate current 28 is a multiple of such drain-source voltage drop and the beta of JFET 21. What's important is gate current 28 is delivered to node 27 and therefore adds to current 29 to become a constituent of load current 30. A final bit of regulation, using the pinch voltage of JFET 22, is provided by JFET 22 having its gate 25 connected to ground. Since the drain-source voltage drop across JFET 22 is relatively small, the resulting gate current of JFET 22 to ground will be small. In other words, the wasted current will be small and the

overall efficiency is improved. Less power is dissipated by circuit embodiments of the present invention to deliver the same power to their regulated loads.

The cited prior art of Taylor does not address this problem nor offer a solution for it. However, Claims 1-20 were drafted so loosely that they could read on Taylor.

The Examiner's indulgence is requested in considering Claims 21-22. Such recite the present invention in a way that distinguishes over the cited prior art.

Support for the circuit of Claim 21 is provided by Specification page 2, lines 25-29, and page 3, lines 3-11, and Fig. 2. Claim 22 is couched as a method for the circuit of Claim 21.

Accordingly, in view of the preceding amendments and remarks, it is respectfully submitted that the pending application, with pending claims 21-22, is in condition for allowance and such action is respectfully requested.

Should the Examiner be of the opinion that a telephone conference with Applicant's attorney would expedite matters, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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